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Design and simulation of 1 Kb memory and its peripherals

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Abstract: **This paper design and simulation of 1Kb memory using memory bank technique. To get required frequency of operation efficient peripherals has to be designed, since the memory core exchanges performance and reliability for diminished area, memory plan depends exceedingly on the peripheral hardware to recuperate both speed and electrical integrity.. In this section we discuss the row decoders, word line drivers, pre-charge circuit, column multiplexers/Decoders, Sense amplifiers and write drivers [14]. Figure1 shows the monolithic peripheral circuitry of 1Kb SRAM Based memory. Generally for Smaller memory designs monolithic architectures are preferred, but in the Design of bigger memories monolithic architecture will not give efficient performance. The frequency of operation of the circuit is reduced by a factor of two as the number of rows doubles. Similarly the frequency of memory, reduced by a factor of four as the number of columns doubles, hence in bigger memory designs memory portioning technique is used which is known as memory banking.**

Keywords**: Architecture, capacitances, delays, monolithic, memory banking.**

1. INTRODUCTION

Depending upon the utilization of a clock, SRAM can be partitioned as synchronous SRAM and asynchronous SRAM. In synchronous SRAM, all the inward flags and timing will be controlled by the clock edge [1]. Information in, control motions and location identifies with the clock signal, it is for the most part utilized as a cache memory while Asynchronous SRAM is autonomous of clock recurrence. All the inner signals and timings are introduced by the placement move. The extent of offbeat SRAM fluctuates from 4 KB to 64 MB. Because of the quick access time of Asynchronous SRAM, it is suitable as main memory for cache less embedded processors which are utilized as a part of modern hardware, estimation of frameworks, organizing hardware [27].

The operation of SRAM can be partitioned into three states, first one is Standby mode, in this mode word line is not initiated, so the address and data lines are kept withdrawn from SRAM memory cells, subsequently cells keep the information as it is and no read and write operation is there. Power consumption during this mode is reduced the foremost. A second mode of operation is reading knowledge from cells. Assume we have a tendency to ae reading knowledge 0 that has already hold on within the memory cell. The Read cycle begins with pre-charging the bit line and bit line bar, after pre-charge operation word line gets actuated as by particular row address and one of the bit line starts discharging through the cell. Here logic 0 is stored in the cell initially, hence Bit line voltage starts discharging through the ground and simultaneously bit line bar voltage starts charging to Vdd. Then sense electronic equipment senses the distinction between the voltages on 2 bit lines and provides correct output, i.e. reads 0 or read 1. If the bit line voltage is greater than the bit line, bar voltage than the output of the sense amplifier as logic 1 which indicates read 1 operation. Similarly if bit line voltage is a smaller amount than bit line bar voltage then output of sense electronic equipment indicate scan 0 Operation [1].

Presence of sense amplifier increases the speed of operation of memory as it senses the small difference between voltages on bit lines otherwise it takes lot of time to perform any read operation. The following method of operation of SRAM is writing data in to the SRAM cell [15].

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Write operation begins with applying knowledge need to be written on bit lines.

Suppose we need to write logic 0, then the bit line will get discharged to 0 and bit line bar voltage is charging to 1. At that point the word line will get actuated, and proper information gets to keep in to the cell.

Peripheral circuitry of SRAM Based Memory

To get required frequency of operation efficient peripherals has to be designed, since the memory core exchanges performance and reliability for diminished area, memory plan depends exceedingly on the peripheral hardware to recuperate both speed and electrical integrity.. In this section we discuss the row decoders, word line drivers, pre-charge circuit, column multiplexers/Decoders, Sense amplifiers and write drivers [15]. Figure 1 shows the monolithic peripheral circuitry of 1Kb SRAM Based memory.

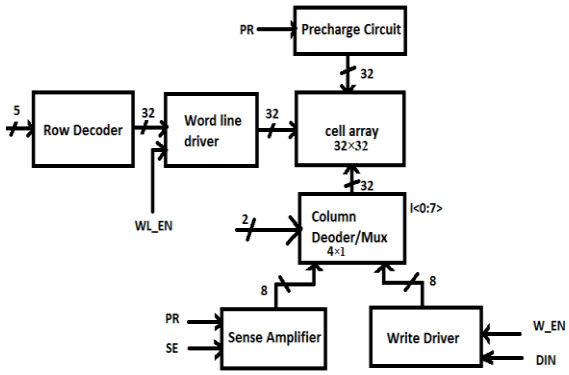

Fig 1: Monolithic Peripheral circuitry of 1Kb SRAM Based Memory [2]

Generally for Smaller memory designs monolithic architectures are preferred, but in the Design of bigger memories monolithic architecture will not give efficient performance. The frequency of operation of the circuit is reduced by a factor of two as the number of rows doubles. Similarly the frequency of memory, reduced by a factor of four as the number of columns doubles, hence in bigger memory designs memory portioning technique is used which is known as memory banking.

Row decoder:

At no matter purpose memory takes into thought absolute address primarily based access address decoders should be on the market.

The Boolean function of the decoder is comparable to 2n n-input AND logic gates, where the extensive fan-in AND operation is actualized in a various levelled structure. The configuration of these decoders has a noteworthy impact on the speed and power dissipation of the memory. Two classes of decoders that is row decoder, whose task is to empower one memory row out of2M, where M is the width of particular fields in address word. While considering these decoders, it is imperative to keep the complete memory floor plan in context.. When the number of inputs is more than or equal to four then the speed of operation of the decoder is effected so pre-decoders are to be used which reduces the large fan-in such that the speed of the decoder is improved. The principal level is the pre-decoder where two groups of address inputs and their complements are first decoded to initiate one of the pre-decoder yield wires separately to obtain the partially decoded outputs. The pre-decoder yields are consolidated at the following level to enable the word line. The decoder delay comprises of word line wire delay, interconnect delay of pre-decoder and gate delays in the critical path. As the wire RC delay develops as the square of the wire length, the wire delays inside the decoder structure, particularly of the word line, gets to be critical in extensive SRAMs.

From delay analysis, it had been ascertained that the NOR decoder is faster than the NAND based decoder.

Monolithic Cell Array:

SRAM cell array size and its introduction are most imperative to consider before the start of circuit configuration. For the outline of bigger memories with specific operating frequency, we have to plan the small blocks of memory which fulfil the frequency prerequisite and numerous utilization of such small blocks will give the bigger memories. Array size can be

defined as the number of rows and columns and the frequency of operation is mainly depends on the number of rows and columns. Frequency of operation is reduced by a factor of two as the number of rows doubles whereas frequency is reduced by a factor of four as the number of columns doubles. Hence, to increase the speed of memory, number of rows and columns are to be decreased.

Word Line Driver:

As word lines have large parasitic capacitance the output of decoder cannot drive the last cell in a memory row. So there must be a buffer exists between decoder and monolithic memory array to drive the last cell in a row. Figure 4 shows the schematic of the everyday word line driver.

It is a circuit which is nothing but the cascading connection of the AND gate with an even number of inverters [15]. To drive the word line which is having a large parasitic capacitance we need to design a stack of inverters with increase in size such that it should capable to drive the worst case cell.

Pre-charge Circuit:

This circuit is used to pre-charging the both bit lines voltages to supply voltage and pre-charging operation should perform before every write and read operation. Figure 3.5 shows the pre-charge circuit which consists of pull up PMOS transistors and an equalizer which is used to equalize the voltage on both bit lines.

The pull up PMOS transistors are controlled by PR signal [9] i.e. The Transistor M3 shown in the schematic of Pre-charge is an equalizer which is used to equalize the voltage on both bit lines. Pre-charge circuit should provide large driving current to drive the bit lines which are having large parasitic capacitances, so the transistor sizes of pre-charge circuit need to be increased.

Sense Amplifier:

Sense Amplifiers plays a crucial role in the design of memories to achieve performance, reliability and functionality of memory circuits. Normally sense amplifiers perform numerous operations like voltage amplification, reduction in delay, power reduction and restoration of original signal.

Generally sense amplifiers are used in the memories to speed up the read operation. Sense amplifier takes the small signal difference bit line voltage as input and gives full swing single ended output [19]. Access time and power consumption of memory is affected by the sense amplifier hence the performance of memory is improved by reducing both sensing delay and power dissipation. When SE is logic low then both bit line voltages are charges to supply voltage, when SE is logic high then sense amplifier is getting ON and one of the bit line voltage discharges to ground via pull down semiconductor device,.

It takes BL and BL' voltages as an input and generates single ended output. When BL voltage is greater than the BL' voltage then current through is increases and simultaneously current through decreases to maintain Iss as a constant, then the drop across is decreases therefore output voltage will increase, which interprets output as the logic 1[27]. Similarly when BL voltage is less than BL' voltage then it indicates output as the logic 0. In this way, Sense amplifier plays a crucial role in the memory read operation.

Write Driver:

The tremendous bit line swing can bring about huge power dissipation in write operation and during read operation, the bit line voltage swing is normally limited to 180mV, and consequently the write cycle will consume around 1/8th additional power than a scan operation.

Initially, before write operation both bit line voltages are charging to supply voltage and the write operation is performed by enabling WR_EN signal. Suppose if we want to write logic 0 in to the memory cell, then the BB line voltage charges to supply voltage VDD and BT line voltage is discharges to lower potential i.e. ground. The data stored in bit line, BT and bit line bar, BB is accessed by enabling word line. The sizing of transistors in write driver is quiet large to provide large driving current[26].

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Column Decoder/Mux:

This circuit is used to select particular column in the memory array.The typical column decoder/Mux in which the outputs of 2 to 4 decoder are used to enable pass transistors. Depending on the output of decoder only of the bit line or bit line bar is selected and the above circuit acts as a 4 to 1 multiplexer. COL_EN signal is employed to alter the column decoder/Mux electronic system. As we discussed earlier the frequency of operation of memory is strongly affected by number of columns as well as number of rows. Hence to maintain good frequency of operation and an aspect ratio of 32×32, we are using DWL (Divide Word line Architecture). Consider the design of 1Kb array, there is totally 32 numbers of SRAM cells present in a cell row and these 32 cells are divided into 4 portions such that the output of SRAM memory is having a size of 8 bits. So 4 to1 multiplexer is used to select one of the portion out of 4 portions. In this way peripherals design plays a vital role in the design

of any memory and efficient peripheral leads to achieve good frequency of operation. In this thesis all the above peripherals are designed and layouts of all circuits are drawn .Pre layout and post layout simulations of all peripherals are performed and a frequency of 8GHz, 1Kb SRAM is designed.

Pre –Charge Circuit:

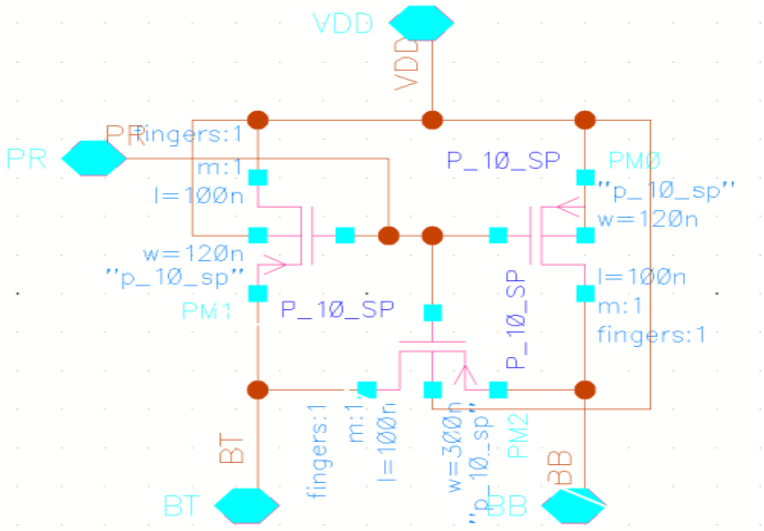

Fig 2: Pre-charge schematic

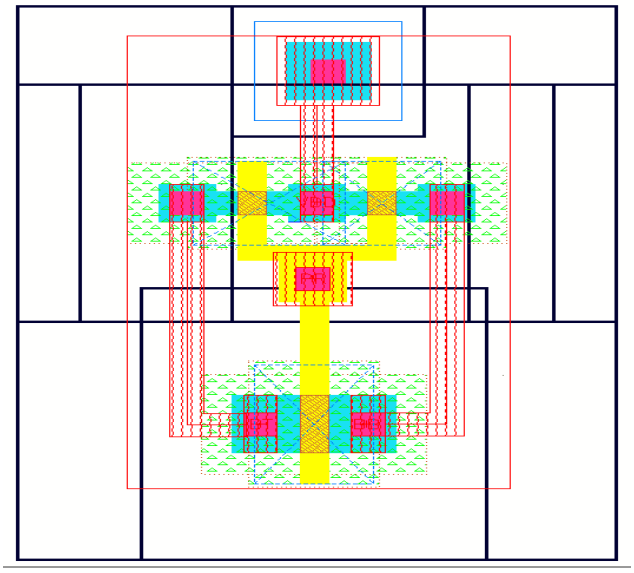

Fig 2.1: Pre-charge layout

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Row decoder:

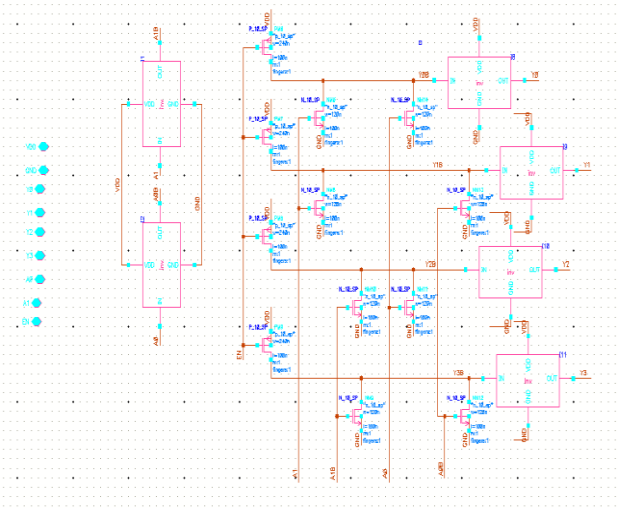

Fig 3: schematic of 2to4 NOR Based Decod

Layout of 2to4 NOR Based Decoder:

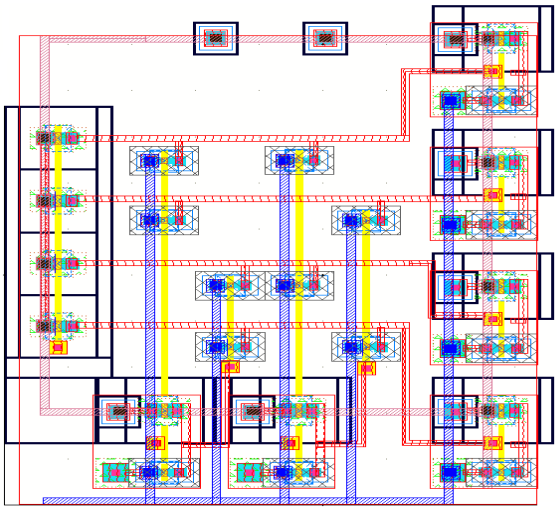

Fig 3.1: Layout of 2to4 NOR Based Decoder

Word line Driver:

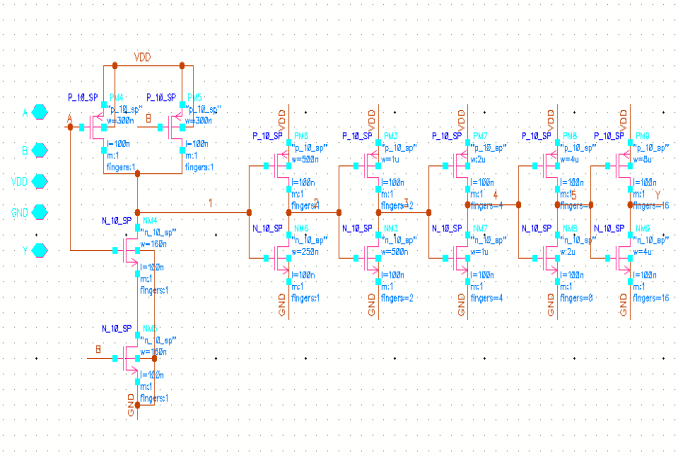

Fig 4: Schematic of Word line Driver

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Sense Amplifier:

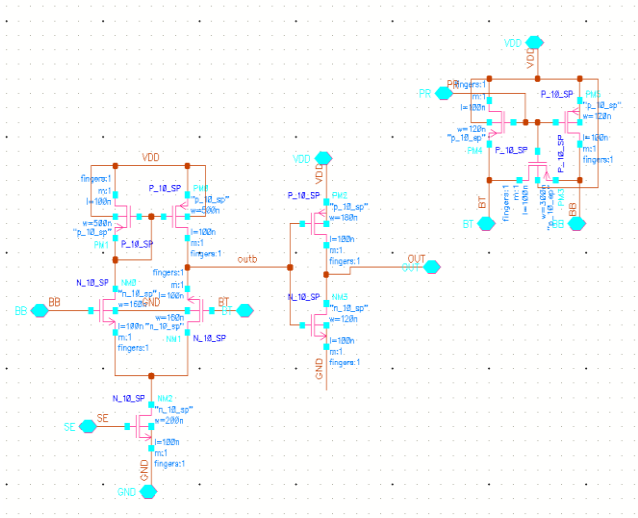

Fig 5: Schematic of Sense Amplifier

Schematic of 1Kb SRAM:

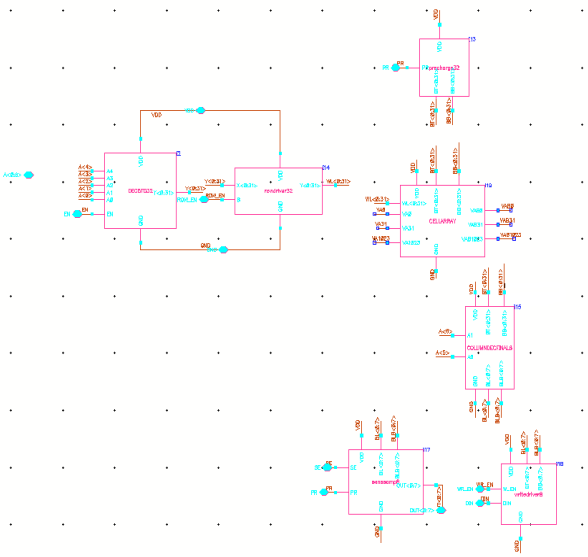

Fig 6: Schematic of 1Kb memory

Simulation results of 1Kb SRAM Memory:

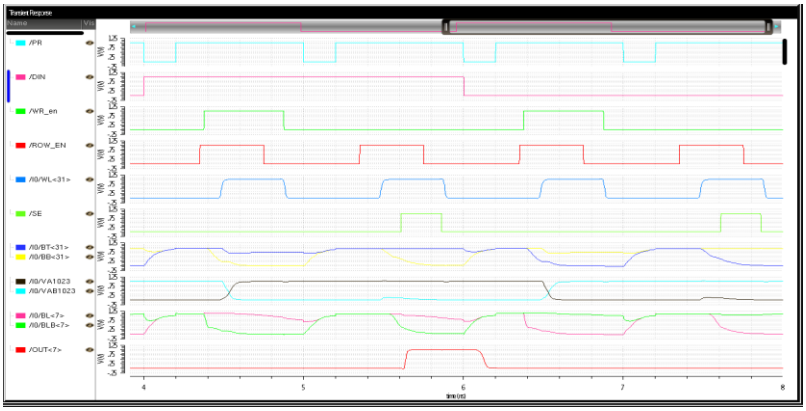

Fig 6.1: Simulation Results of 1Kb memory

Table 1: Power Analysis of 1Kb memory

S.NO.	Description	Pre Layout simulation	Post Layout simulation
1	Write 1 Power	3.522	4.012
2	Read 1 Power	3.448	3.996
3	Write 0 Power	3.523	4.006
4	Read 0 Power	3.533	4.017
5	Total transient power	14.02	16.03
6	Frequency	1.25GHz	1 GHz

2. CONCLUSIONS

In this paper design and simulation of 1kb Memory has been studied. 1-Kb Memory is designed using banking method with data width of 8 bits and Pre layout and post layout simulations of all peripherals are performed and a frequency of 8GHz, 1Kb SRAM is designed.

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